Product/Process Change Notice - PCN 12_0043 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Material Report). Any issues with this PCN or requirements to qualify the change (additional data or samples) must be sent to ADI within 30 days of publication date. ADI contact information is listed below.

PCN Title: AD9910 die revision

Publication Date: 10-Apr-2012

Effectivity Date: 09-Jul-2012 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

Multiple changes, all layers of the silicon were affected slightly:

Die change 1: ESD cells improved

Die change 2: Latch up cells improved

Die change 3: Some of the digital logic was re-routed

Die change 4: REFCLK pass through altered

Spec change 1: CMOS Logic Input Max Current for both Logic 1 increased from 120uA to 150 uA and increased from 50uA to 150uA for Logic 0.

Spec change 2: CMOS Logic Input Typ Current for Logic 0 increased from 38uA to 90uA.

Spec change 3: Full Sleep Mode Max Power increased from 28mW to 40mW.

Reason For Change

Die change 1: Improve ESD sensitivity

Die change 2: Improve reliability

Die change 3: Investigation in the lab and with state of the art digital design timing closure tools verified that multiple hold violations were occurring in the amplitude scale multiplier circuitry. This change fixes these problems.

Die change 4: When "VCO iff" off, but "PLL in" on, the REFCLK is now passed through as an output

Spec changes: correcting errors from original release

Impact of the change (positive or negative) on fit, form, function & reliability

Die change 1: ESD damage is less likely to occur; (improvement).
Die change 2: Latch up is less likely; (improvement).
Die change 3: Has no effect on the AD9910 functionality.
Die change 4: Adds a function that was not present before, (improvement).

Spec change 1: CMOS Logic Input Max Current for both Logic 1 and Logic 0 increased to 150uA.

Spec change 2: CMOS Logic Input Typ Current for Logic 0 increased to 90uA.

Spec change 3: Higher power consumption in full power down mode

Product Identification *(this section will describe how to identify the changed material)*

All material dated after datecode 1227 will be revised silicon.

Summary of Supporting Information

Qualification has been performed per ADI0012, Procedure for Qualification of New or Revised Processes. See attached Qualification Results.

Supporting Documents

Attachment 1: Type: Qualification Report Summary
ADI_PCN_12_0043_Rev_-_AD9910_QUALIFICATION.doc

For questions on this PCN, send email to the regional contacts below or contact your local ADI sales representative					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
AD9910 / AD9910/PCBZ	AD9910 / AD9910BSVZ	AD9910 / AD9910BSVZ-REEL		

Appendix B - Revision History		
Rev	**Publish Date**	**Rev Description**
Rev. -	10-Apr-2012	Initial Release

Analog Devices, Inc. DocId:1865 Parent DocId:1491 Layout Rev:6